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OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
ENGLUND, TERRY LEE	
ART UNIT	**PAPER NUMBER**
2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/601,623	WADA, MASAHARU	
	Examiner	Art Unit	
	Terry L Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06242003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

The drawings are objected to because block 23 of Fig. 2 should indicate the summed currents are equal to 0 as disclosed on page 8, line 1. As presently shown, Fig. 2 appears to be misleading. Since an input of block 22 receives the output (e.g. VOUTA – see corresponding Figs. 3 and 4) of block 21, it is suggested a line be added to Fig. 2 to clearly show the output of block 21 is also coupled to block 22. It is not understood how Fig. 5's circuit "23" actually corresponds to Fig. 2's third circuit "23" since Fig. 5 shows a single output, but Fig. 2 shows two separate outputs from "23". Therefore, several confusing points need to be clarified: 1) Are both outputs of bandgap reference circuit 20/third circuit 23 of Fig. 2 equal to VREFDC? 2) Does Fig. 2's "23" comprise two complete circuits of Fig. 5's "23", wherein Fig. 5's VREFDC (from one circuit) is coupled to Fig. 2's resistor 24, thus placing that resistor in parallel with Fig. 5's resistor 53, and making VREFDC correspond to Fig. 2's V1; and VREFDC (from the other circuit) is coupled to the input of Fig. 2's current mirror circuit 25? 3) Can the two outputs of Fig. 2's blocks 20/23 be provided by two outputs of a current mirror (not shown) with its input being controlled by Fig. 5's VREFDC? A comparison of Figs. 2, 5, and 10 appears to provide some evidence of what the applicants might intend block 23 to comprise of. However, Fig. 5 by itself is misleading with respect to what comprises block "23". It is now believed that block 23 actually comprises two pair of differential transistor pairs (e.g. see first pair 87,88 and second

pair 89,90 shown in Fig. 10). Each pair provides an equal amount of current to its respective output (i.e. to resistor 95 or current mirror 91,92). Therefore, it is suggested Fig. 5 (and its associated description) be modified to clearly indicate the entire circuit in Fig. 5 does not actually represent block "23" as shown. For example, transistors 51,52 of Fig. 5 apparently correspond to only one half of circuit 23, wherein the transistors provide a temperature independent current to resistor 53 (which corresponds to Fig. 2's resistor 24), thus generating first voltage VREFDC (corresponding to Fig. 2's V1). Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: Page 8, lines 3-6 appear to be misleading because they imply one single output current is shared by (or provided

to) both resistor 24 and current mirror circuit 25. However, from the applicants' own figures (e.g. see Figs. 2, and 6), one of ordinary skill in the art would know that two separate output currents are provided by circuit unit 23, wherein only a respective one of the currents is provided to its respective resistor or current mirror circuit. The sum of the voltage description on page 8, lines 18-21 needs clarification because it is not clear if it actually refers to the voltage across resistor 24, or if it refers to V2. For example, only when V2 = VDD/2 would V2 be equal to the voltage across resistor 24. V2 is actually equal to VDD minus (the resistance of resistor 24 times the current flowing through the resistor). The description of Fig. 5 on page 10, line 27 – page 11, line 22 needs to more clearly relate how the single output voltage VREFDC at terminal 54 of circuit unit 23 actually relates to the two output circuit unit 23 shown in Fig. 2 (and again in Fig. 6). For example, is reference potential VREFDC the reference potential both V1 and V2 are actually based on? It is believed the two output terminals of circuit unit 23 (shown in Figs. 2 and 6) actually provide equal amounts of current, instead of the same reference potential. However, if that is the case, why does V1 become stabilized and V2 continues to increase as shown in Fig. 9. Using Fig. 6 as a reference, if the two outputs of circuit unit 23 are providing two equal currents, an increasing current flow through resistor 24 increases voltage V1. However, the current flowing through resistor 26, via current mirror 25, will also be increasing. Therefore, if the current across resistor 24 stabilizes to allow V1 to stabilize, then wouldn't the current through current mirror 25 and resistor 26 also become stabilized, thus allowing V2 to also stabilize? If the two outputs of circuit unit 23 are each the reference potential VREFDC (e.g. as shown in Fig. 5), then V1 is equal to VREFDC. Therefore, the present figures, and their associated descriptions, do not appear to accurately describe the claimed invention as set forth

above. It is suggested the figures and disclosure be carefully reviewed and considered with respect to their accuracy, and appropriate changes and/or clarifications be made to minimize confusion. Appropriate corrections and/or clarifications are required.

Claim Objections

Claims 3-6, 10, 14-17, and 21 are objected to because of the following informalities: It is suggested "current" on line 11 of both claims 3 and 14 be changed to --currents-- to more clearly refer back to the additions of the first/second currents. To improve word flow, it is suggested "a 11^{th}" be changed to --an 11^{th}-- on line 8 of both of claims 10 and 21. Dependent claims carry over any objection(s) from any claim upon which they depend. Appropriate corrections are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Even between the figures and disclosure, this examiner does not understand what the applicants' actually consider a reference potential generation circuit that generates a single reference potential. For example, Fig. 5 shows circuit unit 23 for providing reference potential VREFDC. However, it is not clear how that figure relates to circuit unit 23, shown in Figs. 2 and 6, which are clearly shown with two

separate outputs. For example, are the two outputs currents or voltages? In either case, that does not correspond to a single reference potential, and clarification is requested.

Related to the above, claims 3-6, and 14-17 are further rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for a power-on detector with a reference potential generation circuit which generates a single reference potential (e.g. see Fig. 5), does not reasonably provide enablement for having a band gap reference circuit included in the generation circuit, wherein the band gap reference circuit comprises a third circuit which adds first/second currents to form the single "reference potential" as recited in each of claims 3 (upon which claims 4-6 depend), and 14 (upon which claims 15-17 depend). The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention commensurate in scope with these claims. This problem relates to the confusion with respect to the figures as previously described. As presently understood, the "third circuit" of both claims 3 and 14 actually corresponds to the applicants' "23" shown in Figs. 2, 5, and 6, as well as to 87,88 and 89,90 shown in Fig. 10. However, the claim limitations indicate the third circuit generates a single "reference potential." This apparently implies that the output of the third circuit itself is the "reference potential." If that is the case, how does this relate to the two separate outputs of 23 (e.g. shown in Figs.2 and 6), or to the outputs of 87,88 and 89,90 (shown in Fig. 10)? Are those separate outputs actually equal to one another, as well as to output VREFDC of Fig. 5? If the output of the third circuit is the reference potential, then it is actually the first voltage V1 (e.g. see Figs. 2, 6, and 10). Claims 6 and 17 clearly recite limitations corresponding to the applicants' Fig. 5, wherein the third circuit provides a single reference potential VREFDC. However, as previously described, first/second

voltages V1/V2 are not both based on the same reference potential provided by the third circuit unit. Instead, they are based on separate outputs from the third circuit unit (e.g. see 23 in Figs. 2, 6, and 10).

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicants regard as the invention. Due to the lack of understanding with respect to the present application's figures and disclosure, it is not clear if the first/second voltages recited within independent claims 1 and 11 are actually both based on a single reference potential (as the claims presently imply), based on their own respective reference potential, or each based on a respective current, wherein the currents are of equal value. It is not understood if the reference potential generation circuit actually "includes", or if it is --included in--, a band gap reference circuit as recited within claims 2 and 13. Using the applicants' own Fig 2 as a reference, generation circuit 23 provides at least one type of a reference potential, wherein it is part of band gap reference circuit 20. Therefore, clarification is requested with respect to what the applicants consider their generation and reference circuits. It is not understood how "an output terminal" on line 3 in both of claims 7 and 18 relates to the "reference potential" generated by the reference potential generation circuit of respective claims 1 and 11. For example, does the output terminal provide the reference potential, or are the terminal and potential unrelated? In both claims 8 and 19, line 3 "the output terminal", and lines 8-9 "a voltage across the second load element" are misleading. From the applicants' own figures, it is understood that the first load element (claims 7 and 18)

and the current mirror circuit (claims 8 and 19) are clearly coupled to two separate output terminals, not a single, common output terminal as the claims appear to imply. For example, see the output terminal coupled to first load element (i.e. 24 of Figs. 2 and 6, and 95 of Fig. 10) and another output terminal coupled to a current mirror circuit (i.e. 25 of Figs. 2 and 6, and 91,92 of Fig. 10). It is not clear how the voltages across the first/second load elements in the last three lines of both claims 8 and 19 relate to the first/second voltages recited within their respective independent claim. For example, using the applicants' own Fig. 2 as a reference with respect to "a voltage across the second load element", the second load element corresponds to resistor 26. However, voltage V2 is not actually the voltage across that load element. V2 = VDD – (the resistance of resistor 26 times the current flowing through resistor 26), and this is actually equal to the voltage dropped across the output end of current mirror circuit 25. The use of "seventh MOS transistor of a second conductivity type" on lines 2-3 of each of claims 9 and 20 implies first-sixth MOS transistors, as well as a first conductivity type, wherein those other transistors and the other conductivity type are not identified within either of claim 9's or claim 20's chain of dependency. Similar to claims 7 and 18 above, "an output terminal" on lines 4-5 of both claims 9 and 20 is not clear with respect to its relationship with the "reference potential" generated by the reference potential generation circuit recited within claim 1 (or 11). Line 2 of both claims 10 and 21 recites "a ninth MOS transistor", thus implying first-eighth MOS transistors, which are not identified within either claim's chain of dependency. It is not clear what the reset circuit recited within claim 11 actually refers to. For example, does the overall "power-on reset circuit" actually comprise another type of "reset circuit" within it, or are the data holding circuit, reference potential generation circuit, and first comparator each one part of the reset circuit?

Claim 10 recites the limitation "the output terminal" in line 28 with insufficient antecedent basis for this limitation in the claim. Therefore, does this terminal relate to an overlooked output terminal (i.e. intended but not recited) of the detector, reference potential generation circuit, or the first comparator?

Similar to claim 10 above, claim 20 recites the limitation "the output terminal" in lines 24-25 with insufficient antecedent basis for this limitation in the claim.

Dependent claims carry over any rejection(s) from any claim(s) upon which they depend.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

In so far as being understood, claims 1, 2, and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Sakurai. Fig. 3 comprises reference potential generation circuit M297,M295, M300,R288,Q291 for generating at least one reference potential (e.g. at the gate/drain connection of M297. First comparator Comparator compares first voltage V_{first_down} and second voltage V_{first_up}, wherein both voltages are generated on the basis of the reference potential, and V_{first_down} can also be considered based on first potential supply source gnd (due to the voltage drop across R289,Q292), and V_{first_up} can be considered based on second potential supply source V_{DD}, which is different from gnd (due to the voltage drop across M298,M296, M301). Sakurai discloses that when V_{first_down} is equal to or greater than V_{first_up}, the comparator will output an active low signal V_{ready} (e.g. see column 3, lines 52-55), which one of ordinary

skill in the art would recognize as a means for detecting the power-on condition. Referring to Fig. 2a, this occurs when V_{DD} is at approximately 2.6 volts (understood to be with respect to gnd). Since both V_{first_down} and V_{first_up} are each approximately .56 volts, their sum will be less than the potential difference between V_{DD} and gnd, thus anticipating claim 1. Sakurai discloses the Fig. 3 circuit is related to a bandgap circuit (e.g. see column 3, lines 25-32). Therefore, the reference potential generation circuit can be considered as including a band gap reference circuit, and claim 2 is anticipated. Deeming R289,Q292 as one type of first load element connected between an output terminal (e.g. the common connection between R285 and R289) and first potential supply source gnd, those elements anticipate claim 7 because this load allows first voltage V_{first_down} to be generated.

Claim Rejections - 35 USC § 103

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

In so far as being understood, claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakurai as applied to claim 1 above, and further in view of Suda. As previously described, Sakurai shows and discloses a power-on detector comprising a reference potential generation circuit and a first comparator. However, the reference shows only a common symbol for the comparator in Fig. 3, and therefore does not show/disclose a specific structure. Fig. 1 of Suda shows a conventional comparator. Therefore, it would have been obvious to one of ordinary skill in the art to replace Sakurai's generic type comparator (e.g. no specific structure shown or disclosed) with the known comparator of Suda's Fig. 1, thus rendering claim 10 obvious. [Note: The seven MOS transistors M1,M2,M6,M3,M4,M7,M5 of Suda's comparator correspond to claim 10's first comparator structure comprising ninth – fifteenth MOS transistors, respectively. For example, the ninth – eleventh and the fourteenth MOS transistors are of the first conductivity type (PMOS); the twelfth, thirteenth, and fifteenth transistors are of the second conductivity type (NMOS); VDD is the second potential supply source; GND is the first potential supply source; the gates of the eleventh and fourteenth transistors are coupled in common; and the output terminal OUT is the common connection between the fourteenth and fifteenth transistors.] The use of Suda's specific (but conventional) comparator in place of Sakurai's general type comparator merely uses functionally equivalent components (e.g. a comparator in this case).

In so far as being understood, claims 11-13, 18, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakura, in view of Suda and Iwasaki. Sakurai's Fig. 3 comprises reference potential generation circuit M297,M295,M300,R288,Q291 for generating at least one reference potential (e.g. at the gate/drain connection of M297. First comparator

Comparator compares first voltage V_{first_down} and second voltage V_{first_up}, wherein both voltages are generated on the basis of the reference potential, with V_{first_down} being considered based on first potential supply source gnd (due to the voltage drop across R289,Q292), and V_{first_up} being considered based on second potential supply source V_{DD}, which is different from gnd (due to the voltage drop across M298,M296, M301). Sakurai discloses that when V_{first_down} is equal to or greater than V_{first_up}, the comparator will output an active low signal V_{ready}, which one of ordinary skill in the art would recognize as a means for detecting the power-on condition. Referring to Fig. 2a, this occurs when V_{DD} is at approximately 2.6 volts (understood to be with respect to gnd). Since both V_{first_down} and V_{first_up} are each approximately .56 volts, their sum will be less than the potential difference between V_{DD} and gnd. Sakurai discloses the Fig. 3 circuit is related to a bandgap circuit (e.g. see column 3, lines 25-32), thus the reference potential generation circuit can be considered as including a band gap reference circuit. Elements R289,Q292 are considered one type of first load element connected between an output terminal (e.g. the common connection between R285 and R289) and first potential supply source gnd. The above description closely corresponds to the rejections of the power-on detector with respect to claims 1, 2, and 7 as previously described. However, the reference of Sakurai does not clearly show either the data holding circuit, or the reset circuit as recited within independent claim 11. Fig. 1 of Suda shows a conventional comparator. Therefore, it would have been obvious to one of ordinary skill in the art to replace Sakurai's generic type comparator (e.g. no specific structure shown or disclosed) with the known comparator of Suda's Fig. 1, wherein the use of Suda's specific (but conventional) comparator in place of Sakurai's general type comparator merely uses functionally equivalent components (e.g. a comparator in this case). By interpreting Suda's

Fig 1 comparator in a slightly different manner, transistors M5,M7 can be deemed one type of a reset circuit that responds to the output signal from comparator M1-M4 and M6. Iwasaski shows and discloses data holding circuit 12 being coupled to the output of power-on detector type circuit 5 (e.g. see Fig. 7) to help ensure the data supplied to terminal S is held until the output from circuit 5, applied to terminal R of data holding circuit 12, allows 15 to be reset. Therefore, it would have been obvious to one of ordinary skill in the art to uses Suda's comparator/reset circuit in place of Sakurai's comparator, and output signal V_{ready} would be provided to the reset input of Iwasaki's data holding circuit 12. As previously described with respect to claim 1, and Sakurai's Fig. 2a, once the potential difference between the first/second potential supply sources becomes larger than the sum of the first and second voltages, signal V_{ready} would transition, thus reset circuit M7,M5 (of Suda) would allow the data held by data holding circuit 12 (of Iwasaki) to reset, rendering claim 11 obvious. Suda's comparator/reset circuit is a known structure that can be used in place of Sakurai's generic type comparator, and Iwasaki's data holding circuit 12 is one known type of circuit coupled to the output of a power-on detector type circuit, which will only allow the held data to be reset when the power-on detector type circuit ensures the first/second potential supply sources have reached a predetermined level that would allow other circuitry to operate properly. Since data holding circuit 12 of Iwasaki is disclosed as one type of latch circuit (e.g. see its Fig. 7 label, and its associated structure shown in Fig. 9), claim 12 is rendered obvious. Sakurai's circuit is associated with a bandgap circuit, as previously described, rendering claim 13 obvious. First load element R289,Q292 renders obvious claim 18. The seven MOS transistors M1,M2,M6,M3,M4,M7,M5 of Suda's comparator respectively correspond to claim 20's structure of the first comparator that comprises ninth – fifteenth MOS transistors. For

example, the ninth – eleventh and the fourteenth MOS transistors are of the first conductivity type (PMOS); the twelfth, thirteenth, and fifteenth transistors are of the second conductivity type (NMOS); VDD is the second potential supply source; GND is the first potential supply source; the gates of the eleventh and fourteenth transistors are coupled in common; and the output terminal OUT is the common connection between the fourteenth and fifteenth transistors. Therefore, claim 21 is also rendered obvious.

No claim is allowable as presently written.

Allowable Subject Matter

However, claims 8-9, and 19-20 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. For example, if the "reference potential", "output terminal", and "voltage across" related limitations are clarified satisfactorily, there is presently no strong motivation to modify or combine any prior art reference(s) to ensure the circuit also comprises the relationships between the current mirror circuit and the second load element as recited within claims 8 (upon which claim 9 depends) and 19 (upon which claim 20 depends).

Prior Art

The other prior art references cited on the accompanying PTO-892 are deemed relevant to at least sections of the claimed invention. Fig. 8 of Bando et al. shows a power-on detector comprising a reference potential generation circuit 48 for generating reference potential(s) ND04(V1),ND05(V2); and first comparator 46 for comparing first/second voltages ND06(V3)/ ND07(V4) which are based on the reference potential(s), as well as the first/second potential

supply sources VSS/VC. Yu et al. shows circuitry in Fig. 1 that corresponds to the applicants' own Figs. 3 and 4. For example, Yu et al.'s section 11 corresponds to first circuit 21 shown in the applicants' Fig. 3; Yu et al.'s sections 21,31 (minus transistor 33) correspond to second circuit 22 of the applicants' Fig. 4; and transistor 33 of Yu et al. corresponds to transistor 52 of third circuit 23 shown in the applicant's Fig. 5. Therefore, all of these references should be carefully reviewed and considered.

The prior art references cited on the IDS submitted Jun 24, 2003 were reviewed and considered. None of the references clearly show or disclose first/second voltages based on the same reference potential provided by a reference potential generation circuit as recited within the independent claims.

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund

16 July 2004

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800